**Assignment 5**

**Assignment** All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded ‘0’ marks.

1. Verilog code and testbench for 2-to-4 decoder using data flow modeling with active high enable and active low outputs.

**Ans: Link1:** [**https://www.edaplayground.com/x/7AU3**](https://www.edaplayground.com/x/7AU3)

1. Verilog code and testbench for 3-to-8 decoder using structural modeling (use 2-to-4 decoders as blocks).

**Ans: Link2:** [**https://www.edaplayground.com/x/cajn**](https://www.edaplayground.com/x/cajn)

1. Write the Verilog code and testbench for 3:8 decoder using behavioral modeling. (Hint: use **case** statements)

**Ans: Link3:** [**https://www.edaplayground.com/x/7Dgj**](https://www.edaplayground.com/x/7Dgj)

1. Write the Verilog code and testbench for 8:3 encoder using behavioral modeling. (Hint: use **case** statements)

**Ans: Link4:** [**https://www.edaplayground.com/x/hLbP**](https://www.edaplayground.com/x/hLbP)

**Self-Practice and self-evaluation**

1. Name the gates that can be used as one-bit comparators.

2. What external gate would have been used if the IC were to be active high?

3. Are the outputs of the decoder active low or active high?

4. Find out about the functionality of 74138 and 74139 decoder ICs?

5. If the decoder had been internally constructed using AND gates, what external gate would be required to use the decoder as a Boolean function implementer.

6. Define synthesis. What is the need for synthesis?

7. Why comparators are called iterative circuits? Name some other iterative circuits.

8. How can magnitude comparators be used in memory decoding?

9. Write the behavioral description of a 4-bit magnitude comparator in Verilog.